FIG. 1

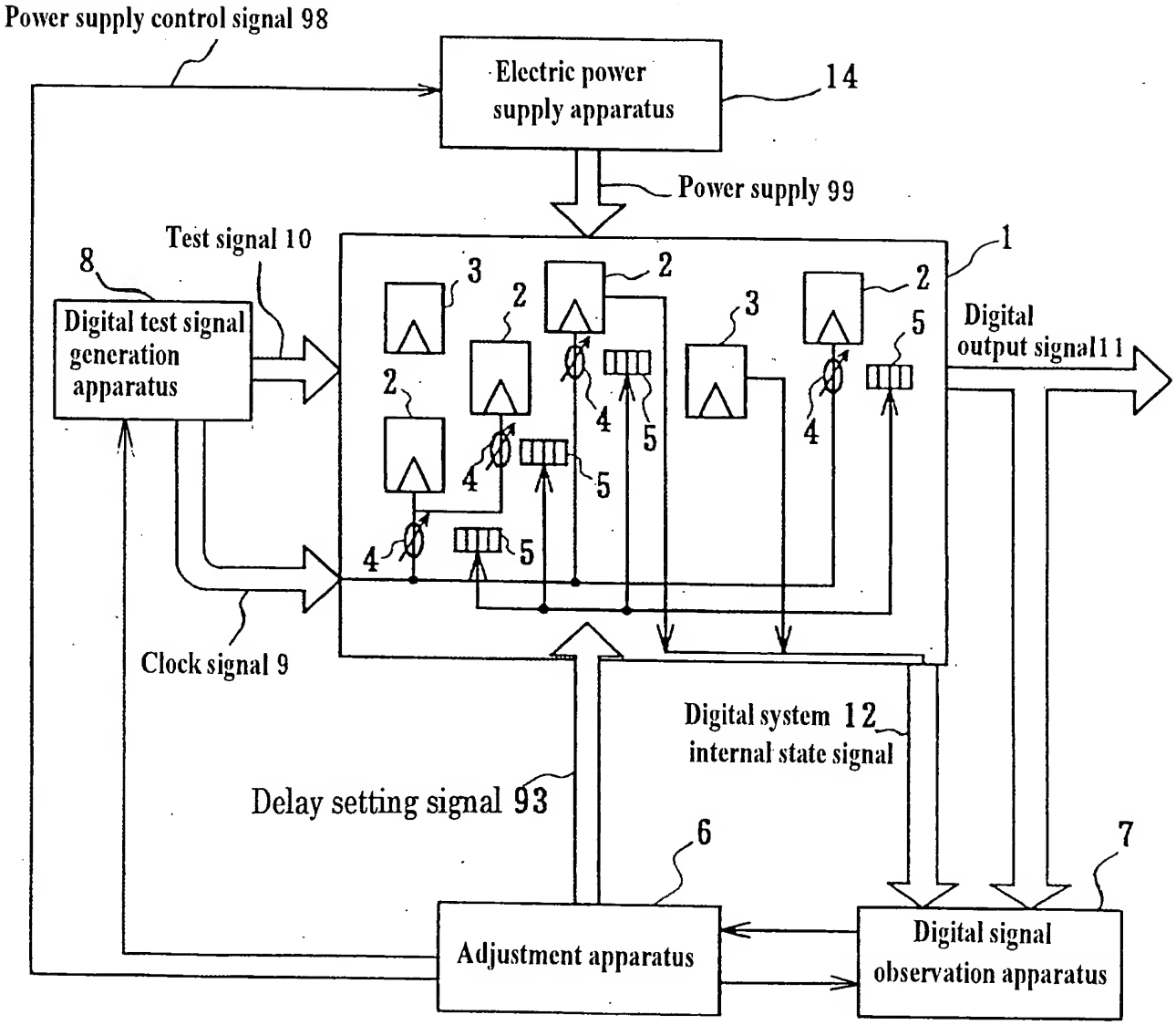

Power supply control signal 98
Electric power supply apparatus
14
Power supply 99
Test signal 10
8
Digital test signal generation apparatus
1
Digital output signal 11
Clock signal 9
Digital system 12 internal state signal
Delay setting signal 93
6
7
Adjustment apparatus
Digital signal observation apparatus

FIG. 2

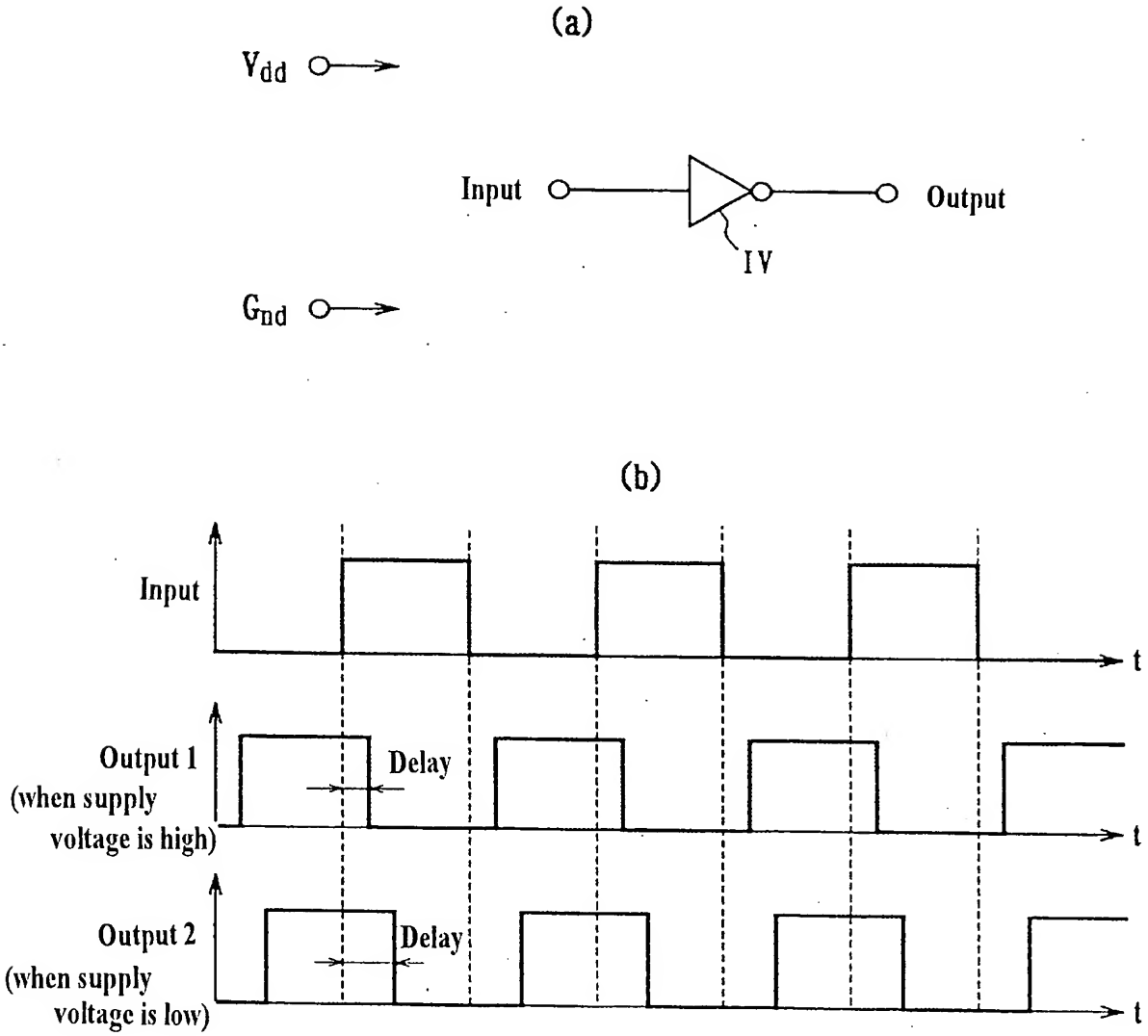

(a)
Vdd
Input
Output
IV
Gnd
(b)
Input
t
Output 1
(when supply
voltage is high)
Delay
t
Output 2
(when supply
voltage is low)
Delay
t

FIG. 3

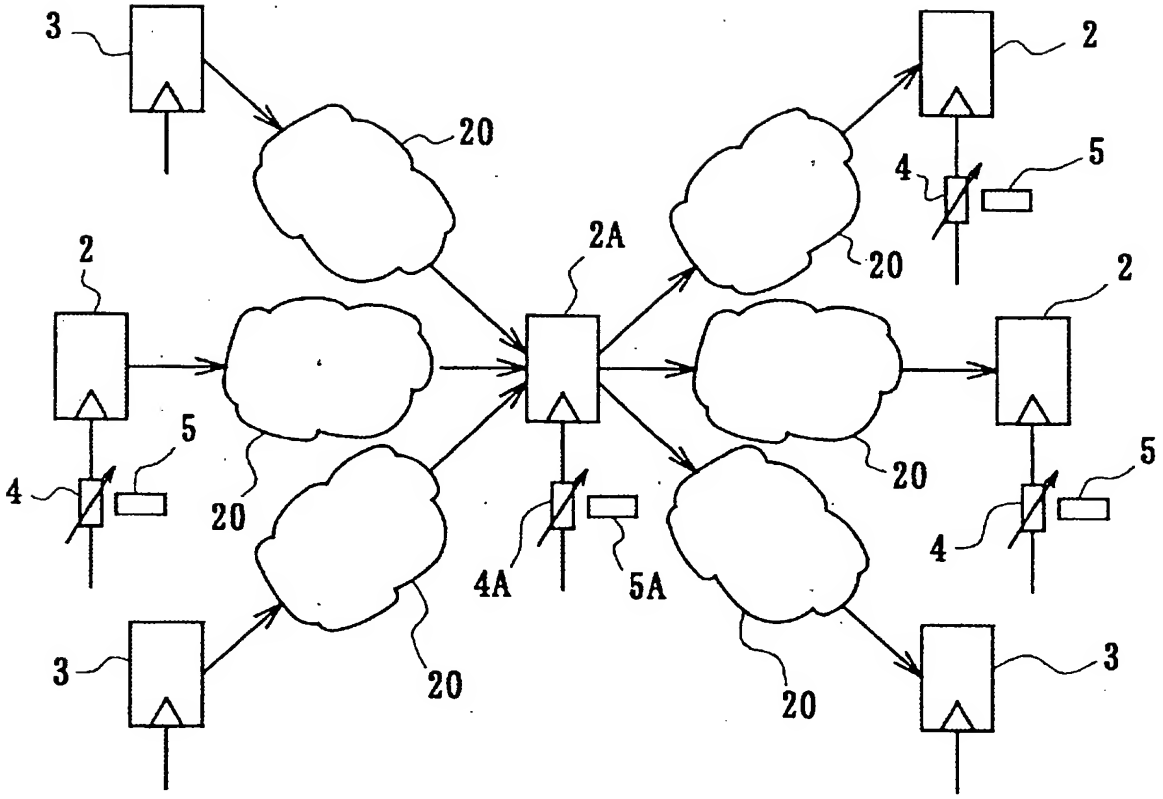


FIG. 4

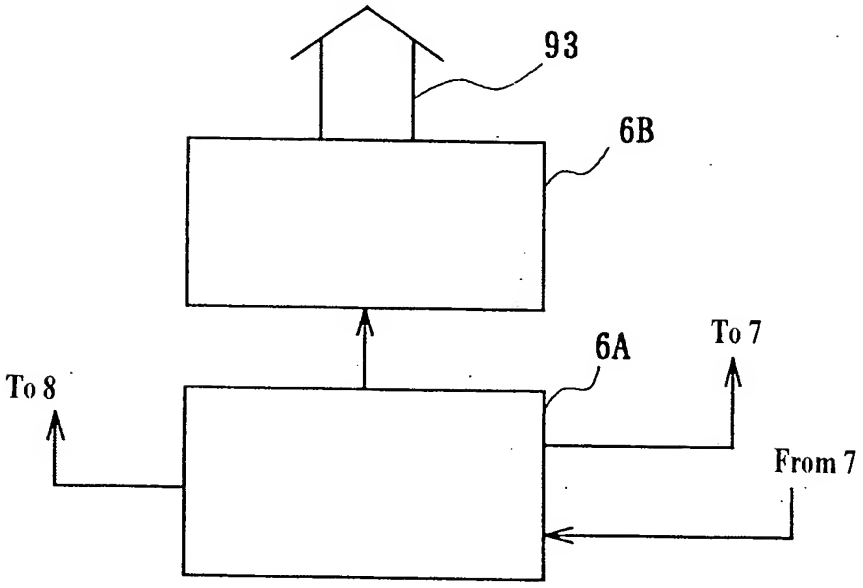


FIG. 5

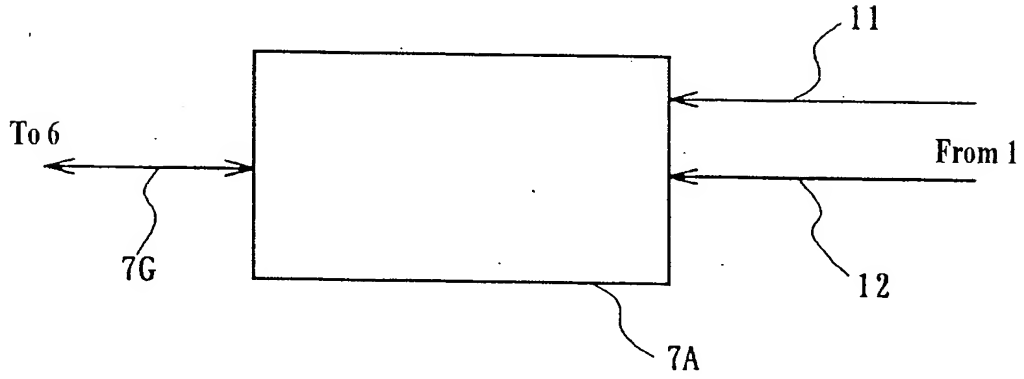


FIG. 6

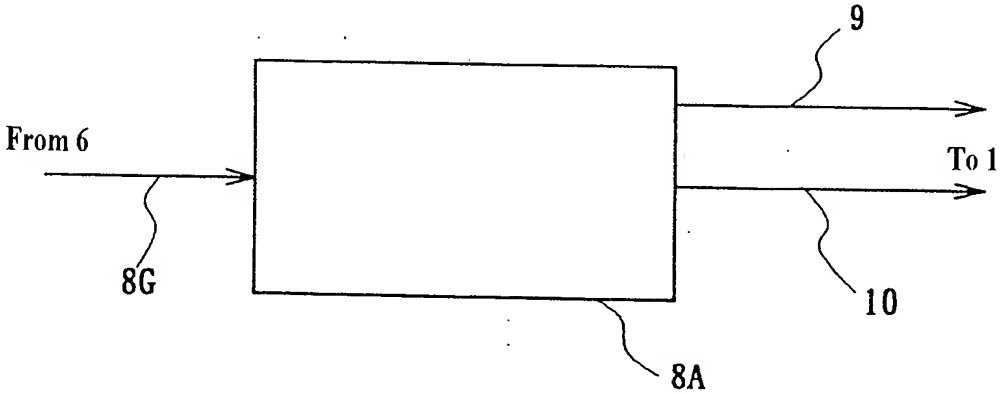


FIG. 7

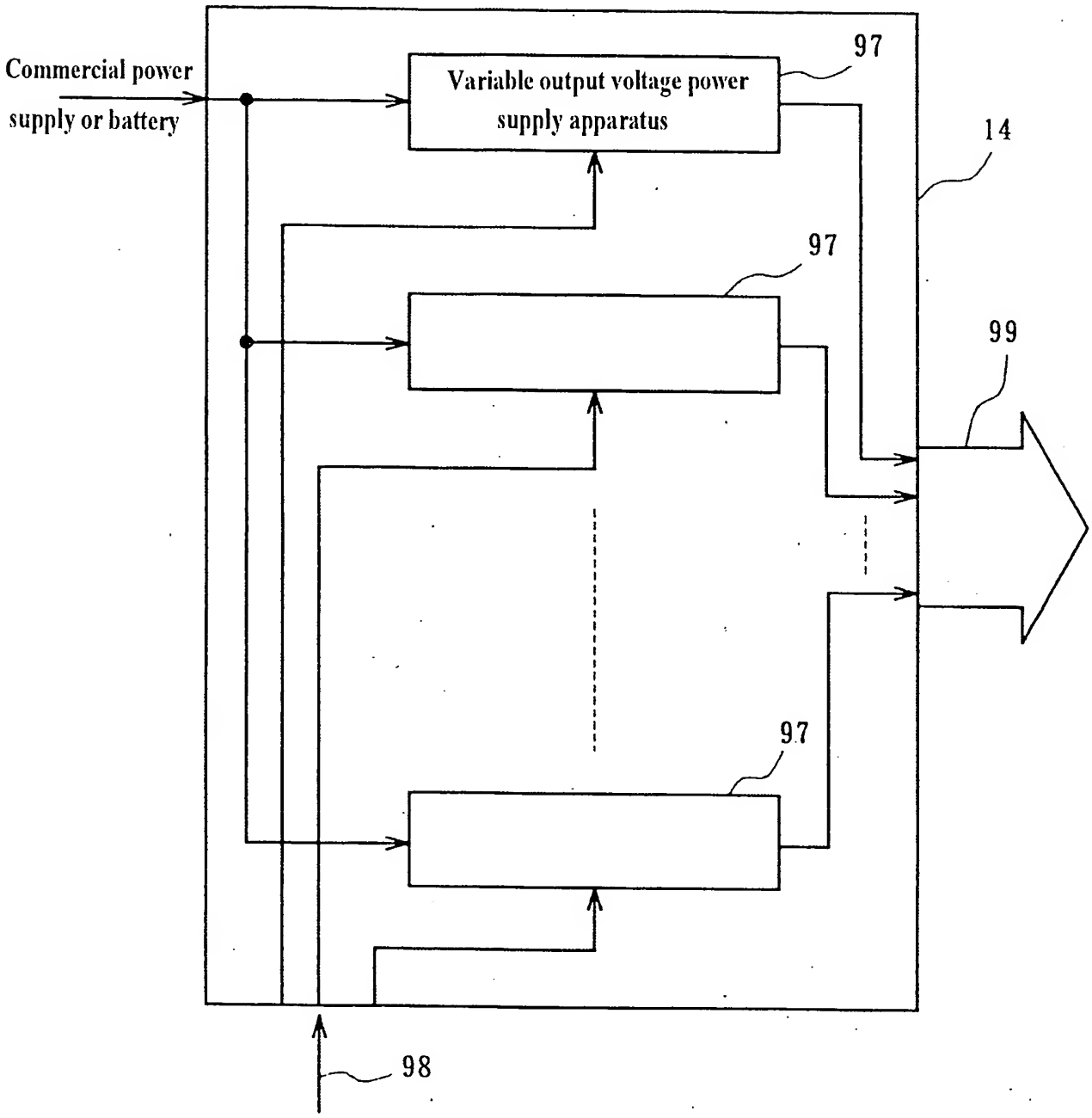

Commercial power
supply or battery
Variable output voltage power
supply apparatus
97
97
97
14
99
98

FIG. 8

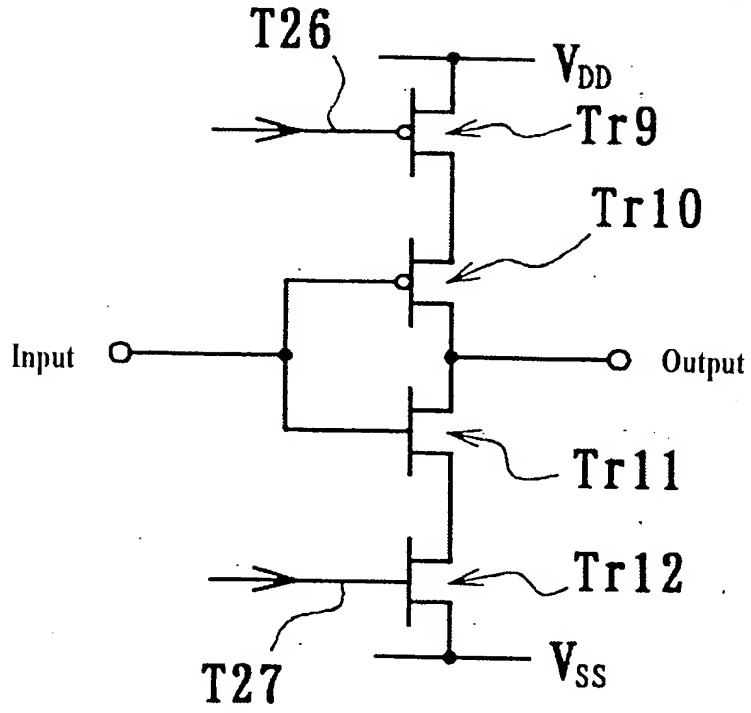

T26
V_{DD}
Tr9
Tr10
Input
Output
Tr11
Tr12
T27
V_{SS}

FIG. 9

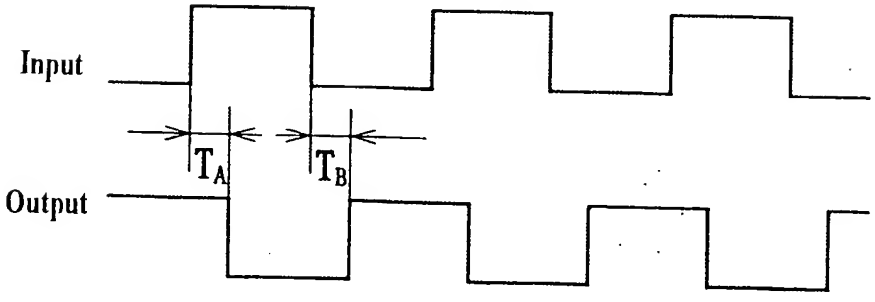

Input
T_A
T_B
Output

FIG. 10

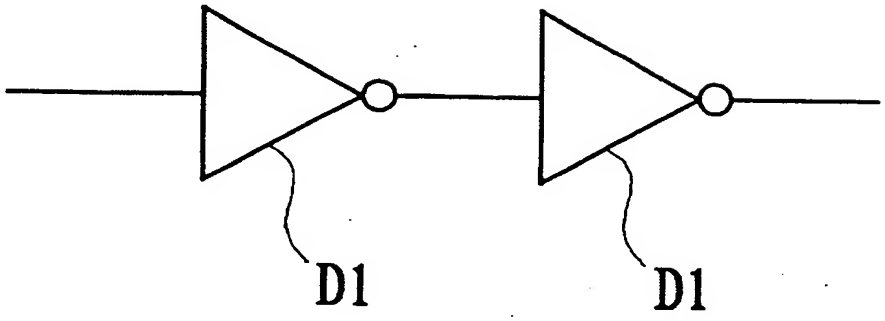


FIG. 11

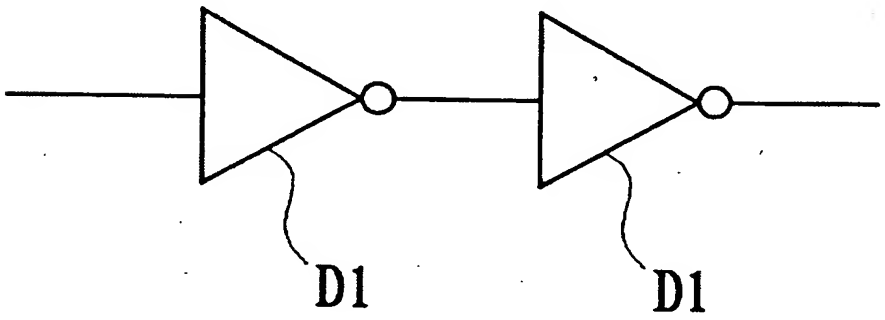


FIG. 12

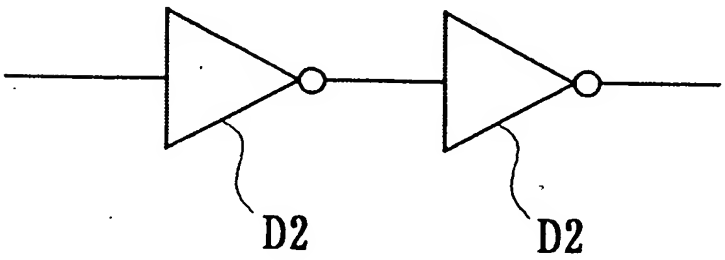


FIG. 13

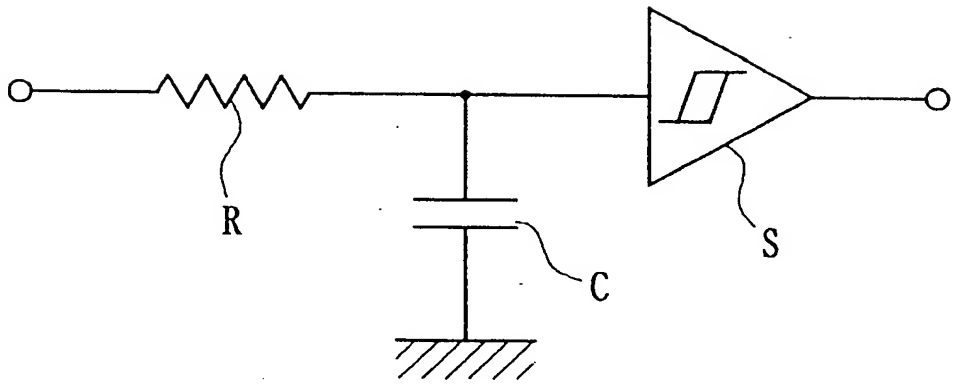


FIG. 14

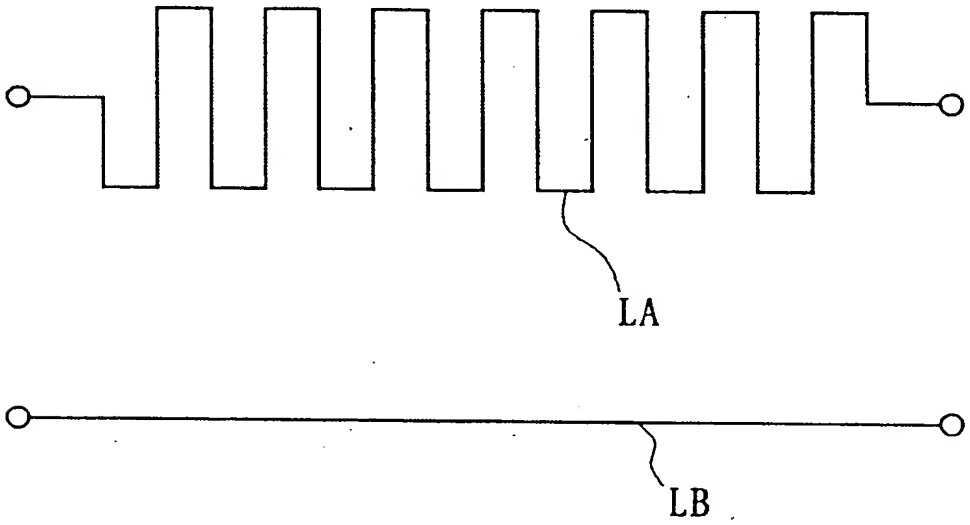


FIG. 15

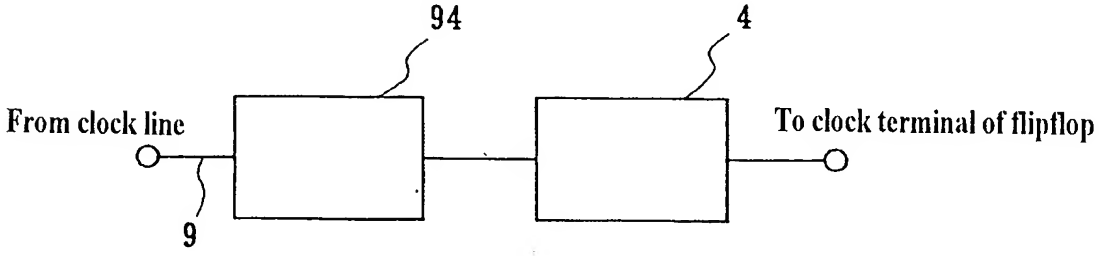


FIG. 16

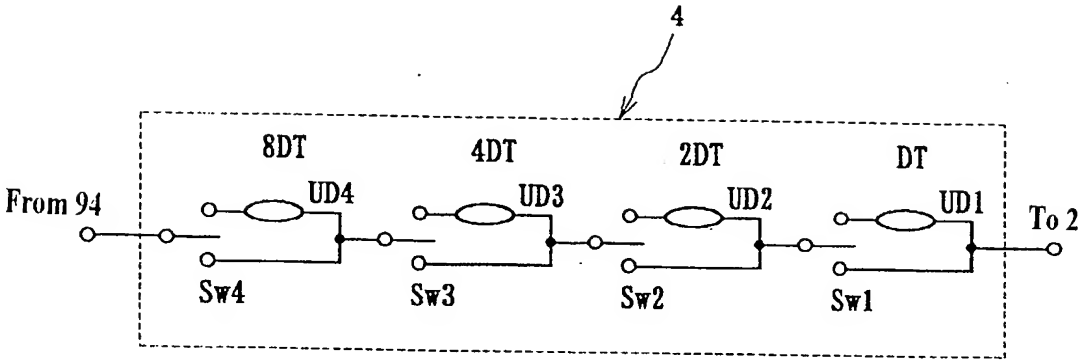

4
8DT
4DT
2DT
DT
From 94
UD4
UD3
UD2
UD1
To 2
Sw4
Sw3
Sw2
Sw1

FIG. 17

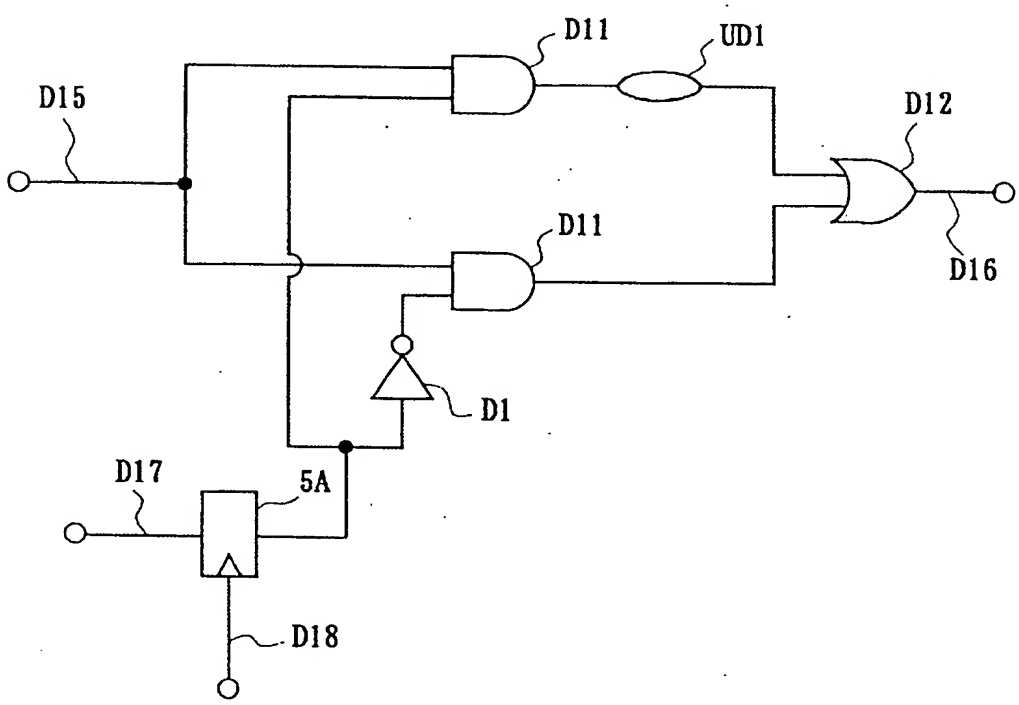

D11
UD1
D15
D12
D11
D16
D1
D17
5A
D18

FIG. 18

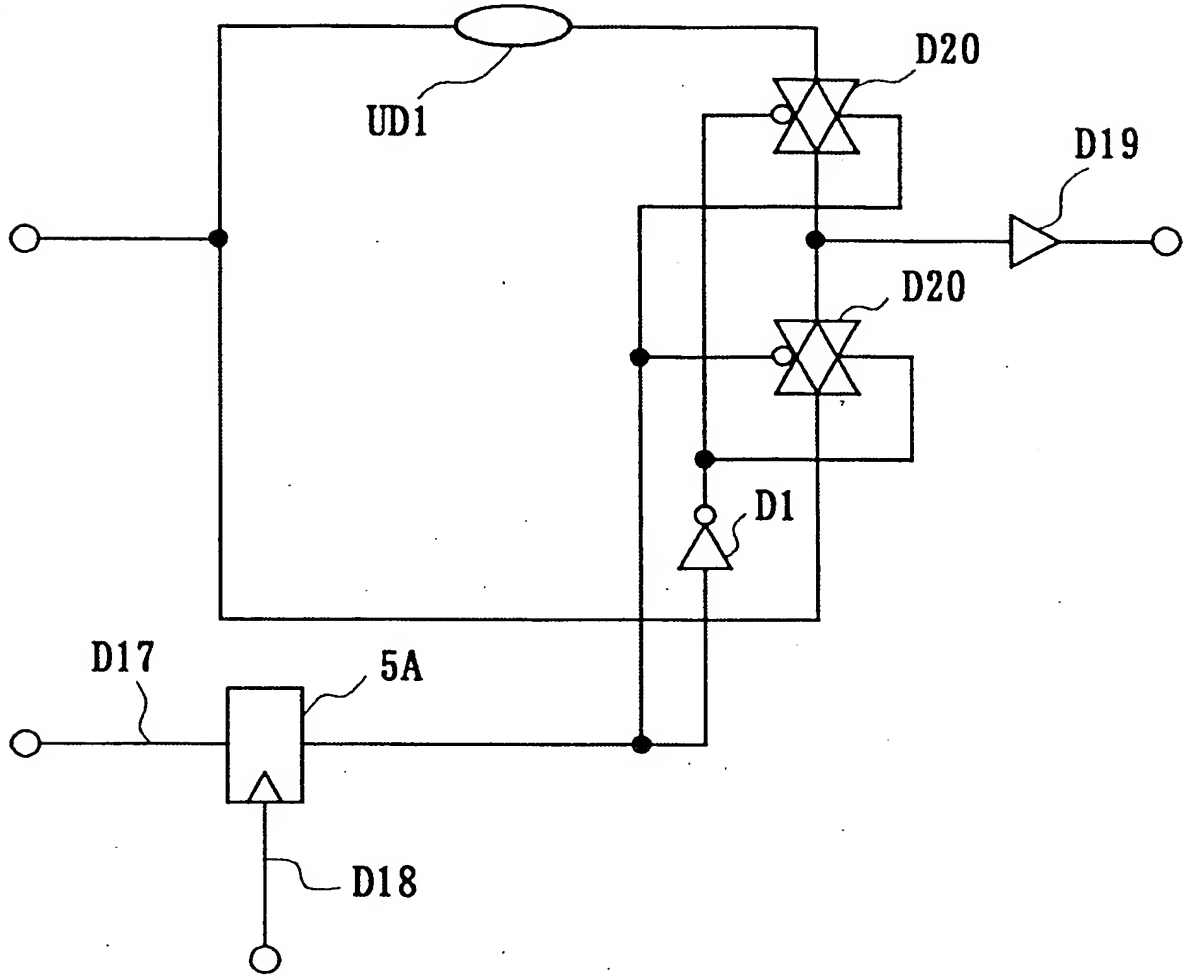


FIG. 19

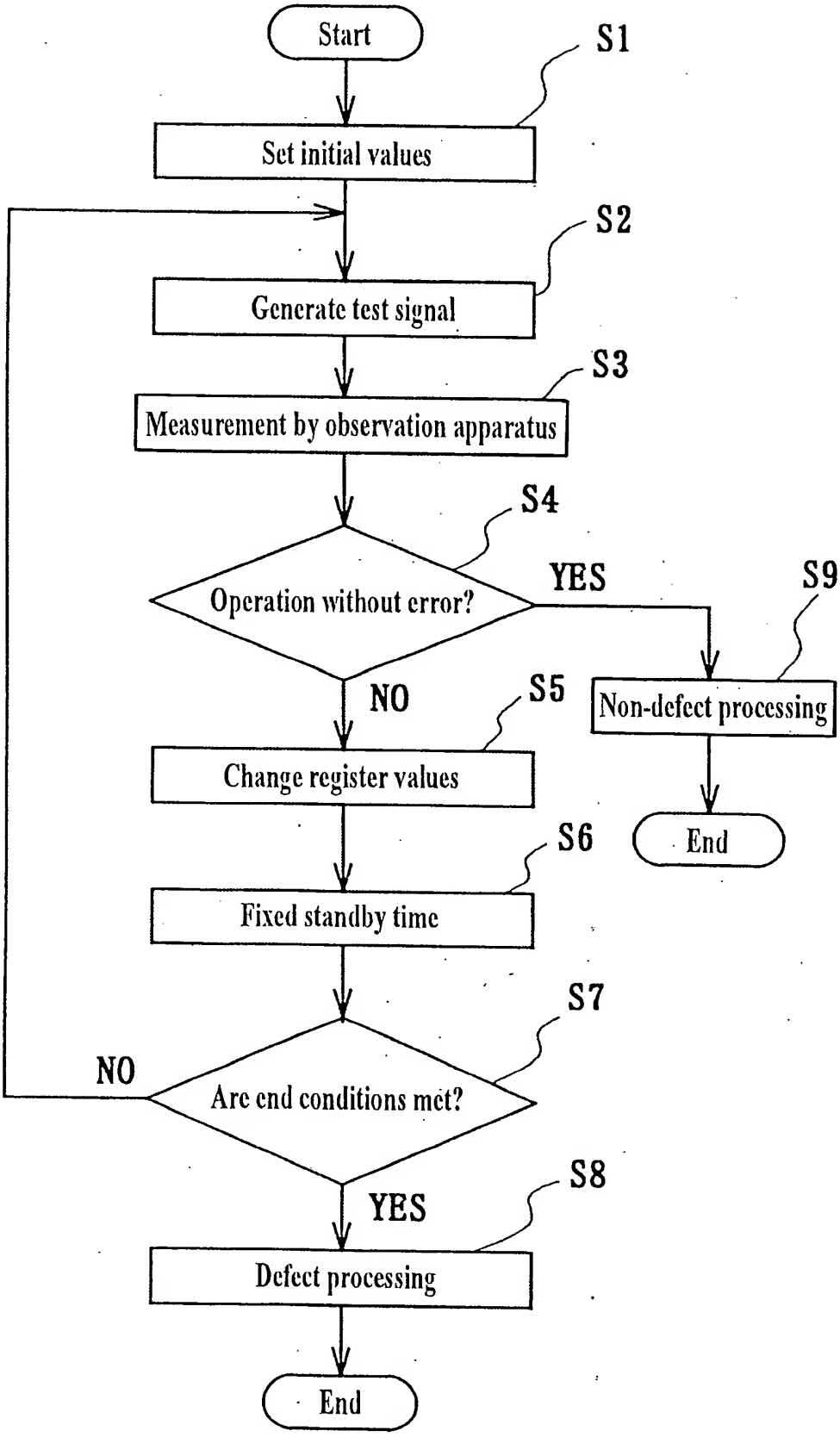

Start
S1
Set initial values
S2
Generate test signal
S3
Measurement by observation apparatus
S4
Operation without error?
YES
S9
Non-defect processing
End
NO
S5
Change register values
S6
Fixed standby time
S7
Are end conditions met?
NO
YES
S8
Defect processing
End

FIG. 20

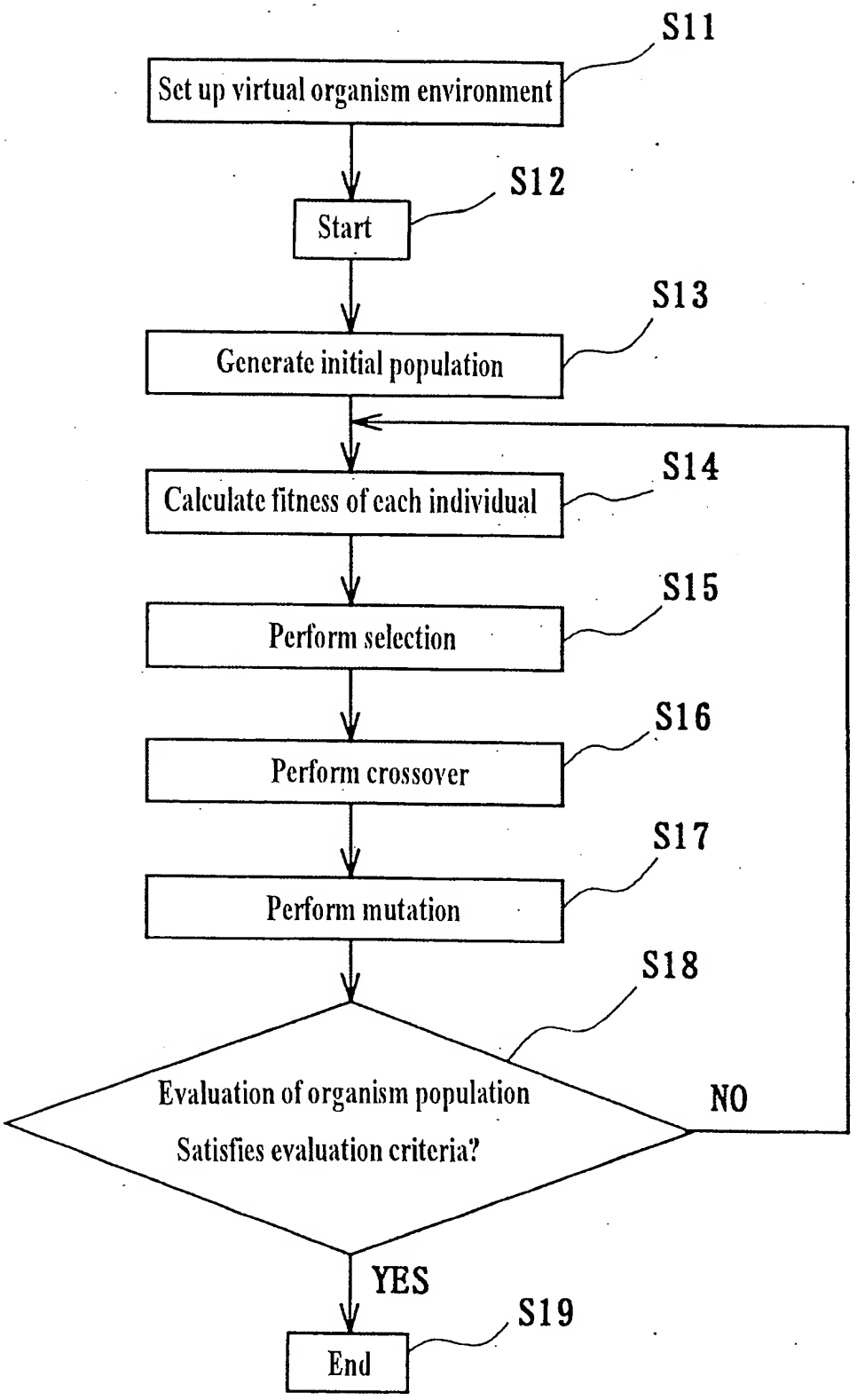

S11
Set up virtual organism environment
S12
Start
S13
Generate initial population
S14
Calculate fitness of each individual
S15
Perform selection
S16
Perform crossover
S17
Perform mutation
S18
Evaluation of organism population
Satisfies evaluation criteria?
NO
YES
S19
End

FIG. 21

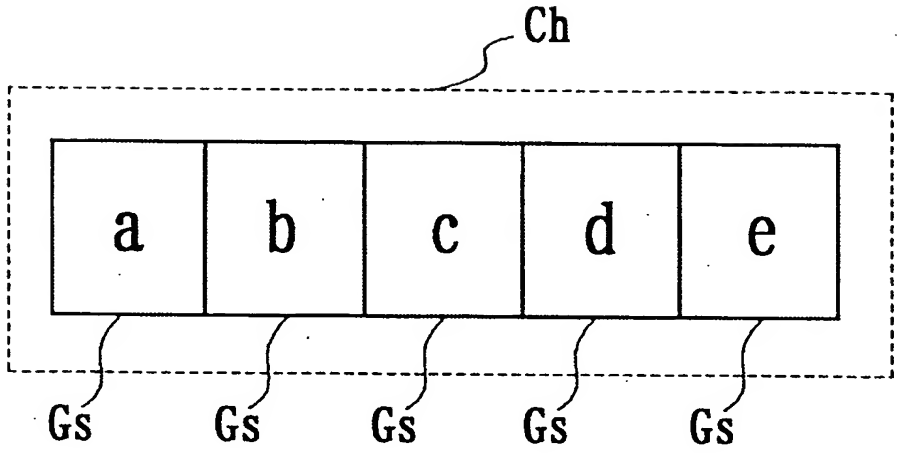


FIG. 22

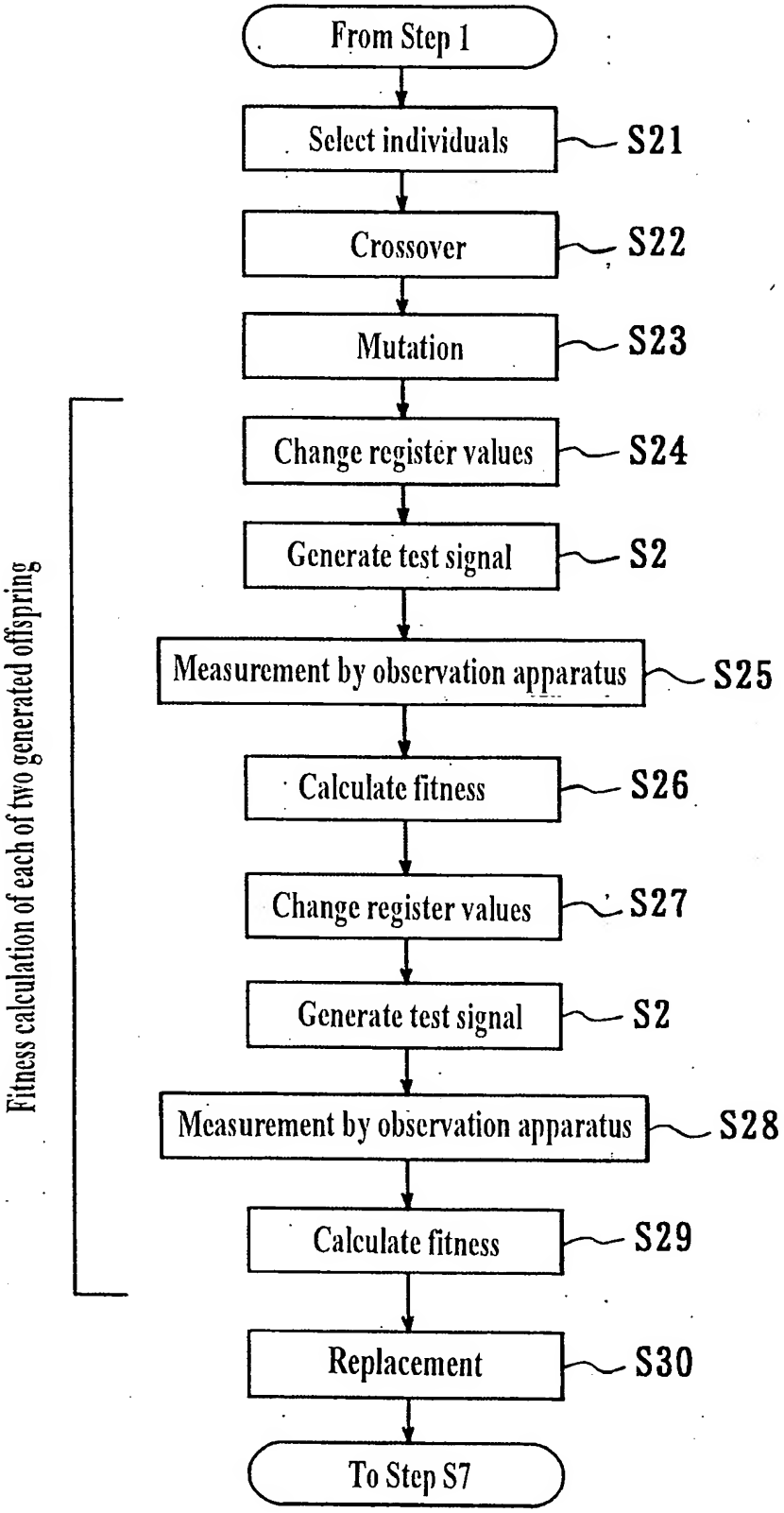
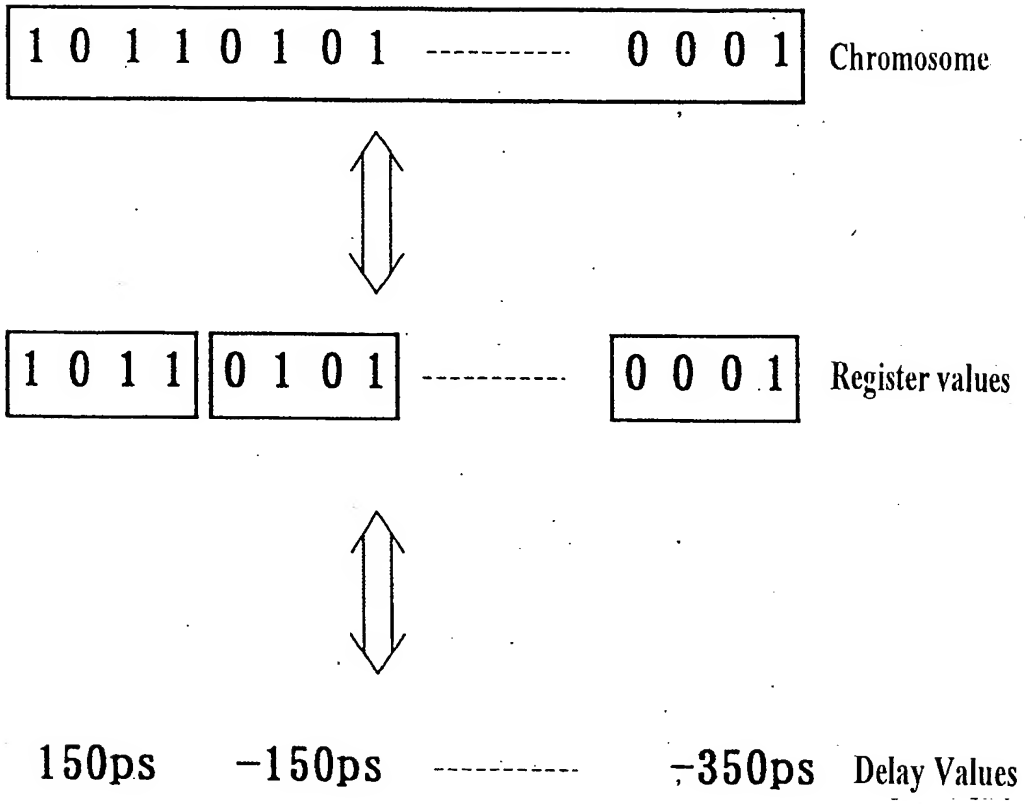

From Step 1
Select individuals
S21
Crossover
S22
Mutation
S23
Change register values
S24
Generate test signal
S2
Measurement by observation apparatus
S25
Calculate fitness
S26
Change register values
S27
Generate test signal
S2
Measurement by observation apparatus
S28
Calculate fitness
S29
Replacement
S30
To Step S7
Fitness calculation of each of two generated offspring

FIG. 23


1 0 1 1 0 1 0 1 ---------- 0 0 0 1
Chromosome
1 0 1 1
0 1 0 1
----
0 0 0 1
Register values
150ps
-150ps

-350ps
Delay Values

FIG. 24

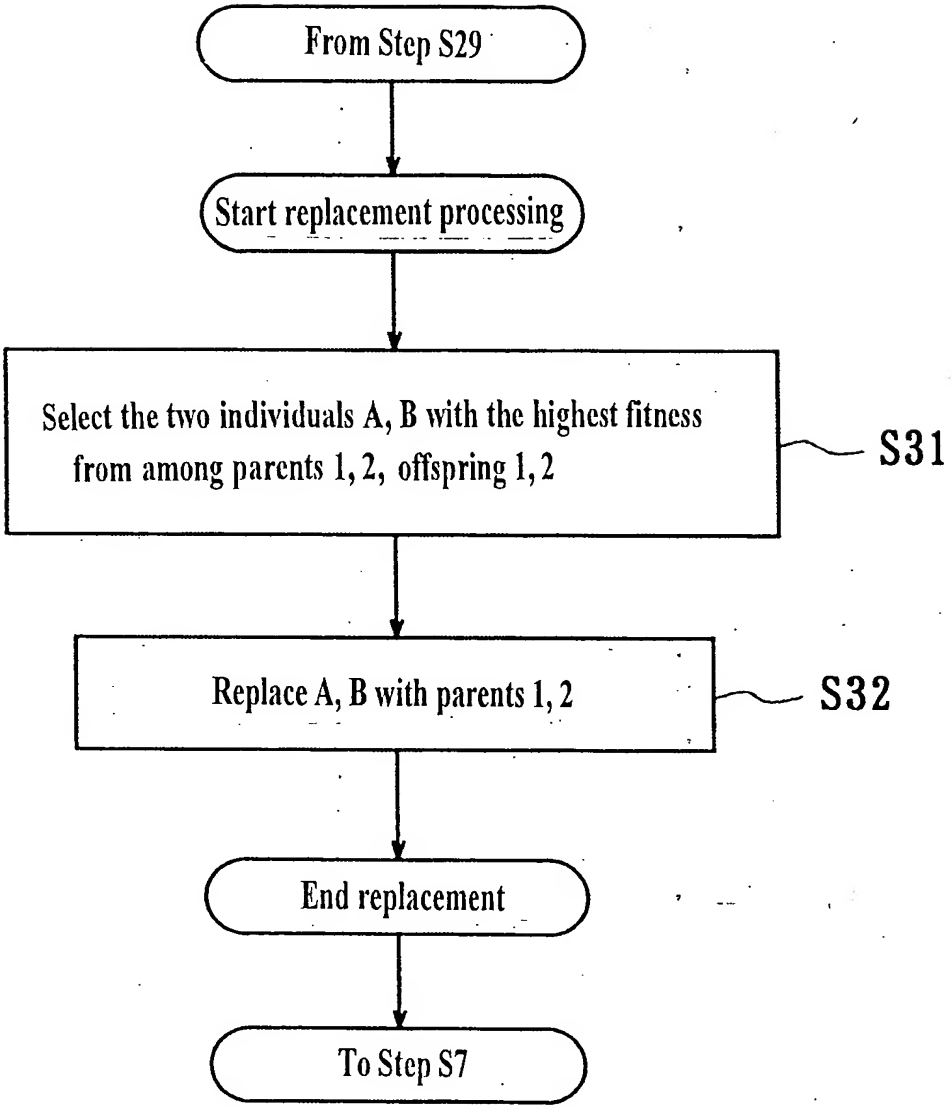

From Step S29
Start replacement processing
Select the two individuals A, B with the highest fitness from among parents 1, 2, offspring 1, 2
S31
Replace A, B with parents 1, 2
S32
End replacement
To Step S7

FIG. 25

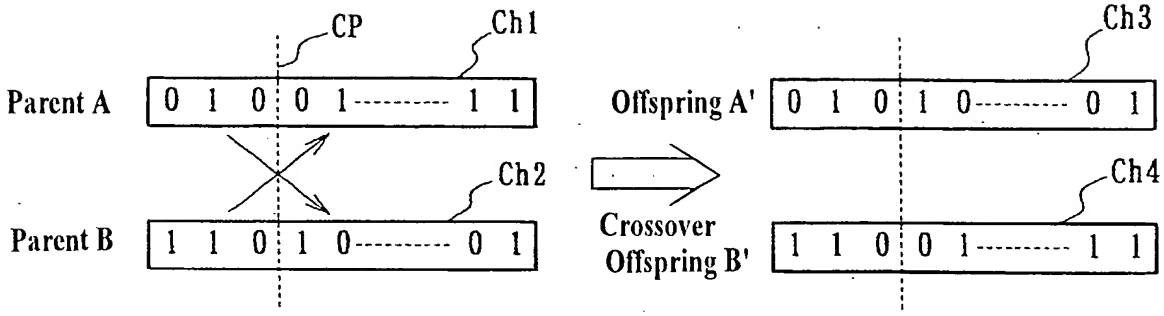

CP
Ch1
Parent A
0 1 0 0 1 1 1
Ch2
Parent B
1 1 0 1 0 0 1
Crossover
Offspring B'
Ch3
Offspring A'
0 1 0 1 0 0 1
Ch4
1 1 0 0 1 1 1

FIG. 26

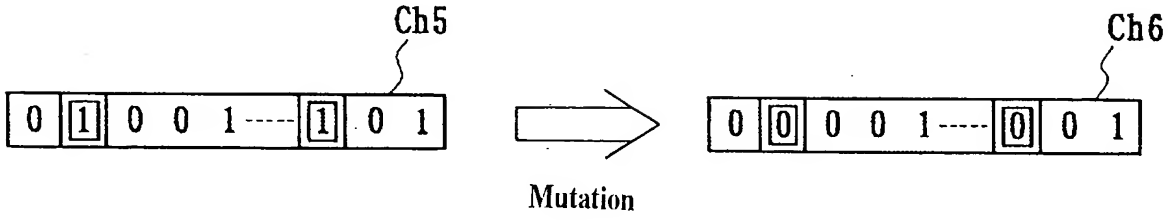

Ch5
0 1 0 0 1 1 0 1
Mutation
Ch6
0 0 0 0 1 0 0 1

FIG. 27

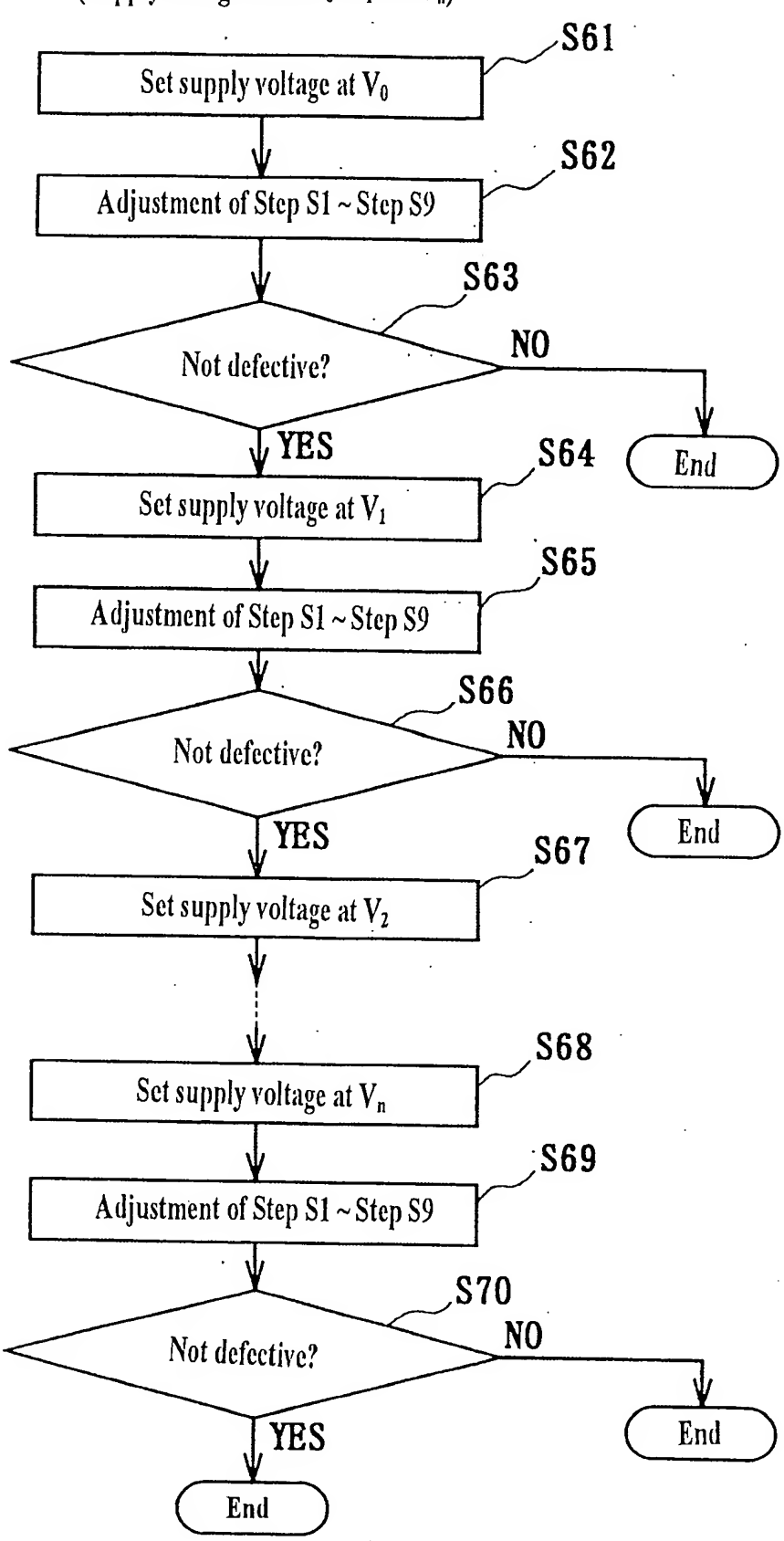

(Supply voltage value V_0>V_1>...>V_n)
S61
Set supply voltage at V_0
S62
Adjustment of Step S1 ~ Step S9
S63
Not defective?
NO
End
YES
S64
Set supply voltage at V_1
S65
Adjustment of Step S1 ~ Step S9
S66
Not defective?
NO
End
YES
S67
Set supply voltage at V_2
S68
Set supply voltage at V_n
S69
Adjustment of Step S1 ~ Step S9
S70
Not defective?
NO
End
YES
End

FIG. 28

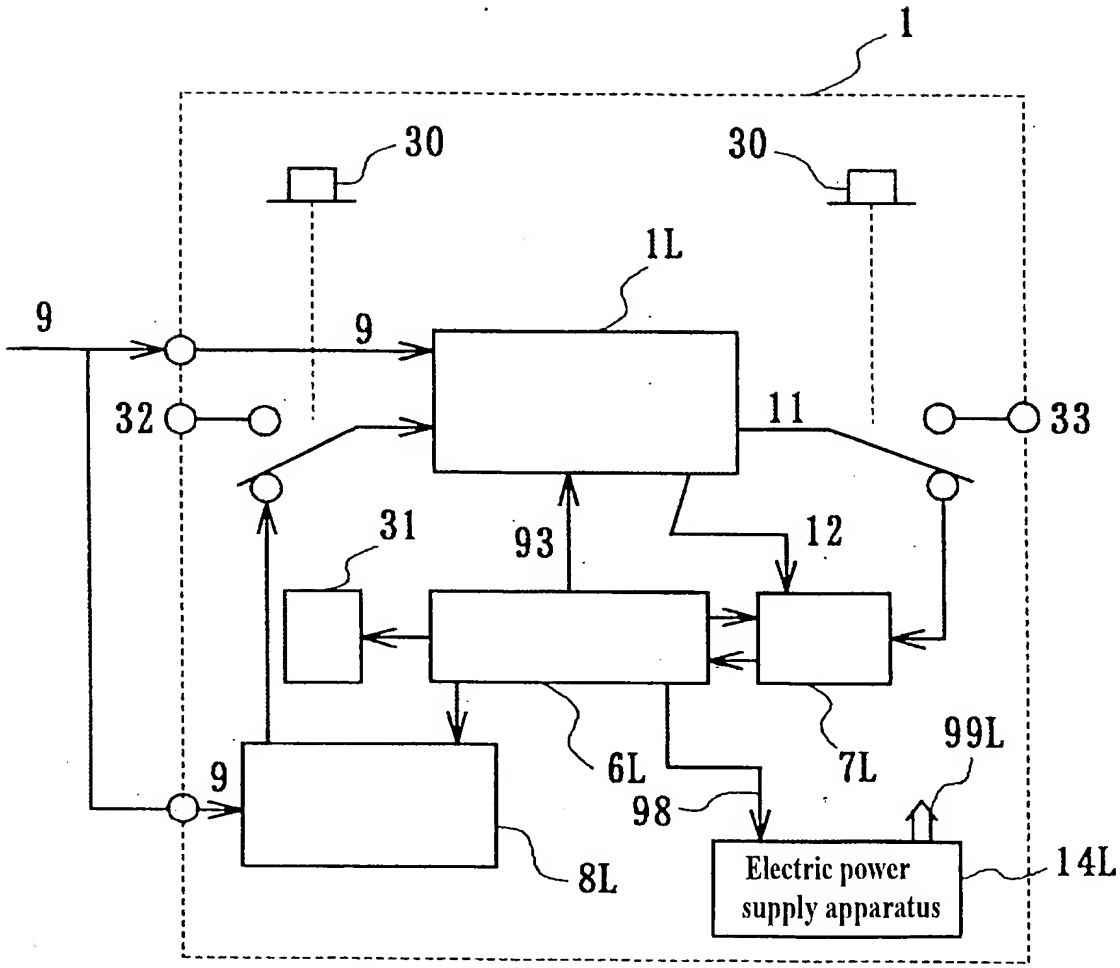

1
30
30
1L
9
9
32
11
33
31
93
12
6L
7L
99L
9
98
8L
Electric power supply apparatus
14L

FIG. 29

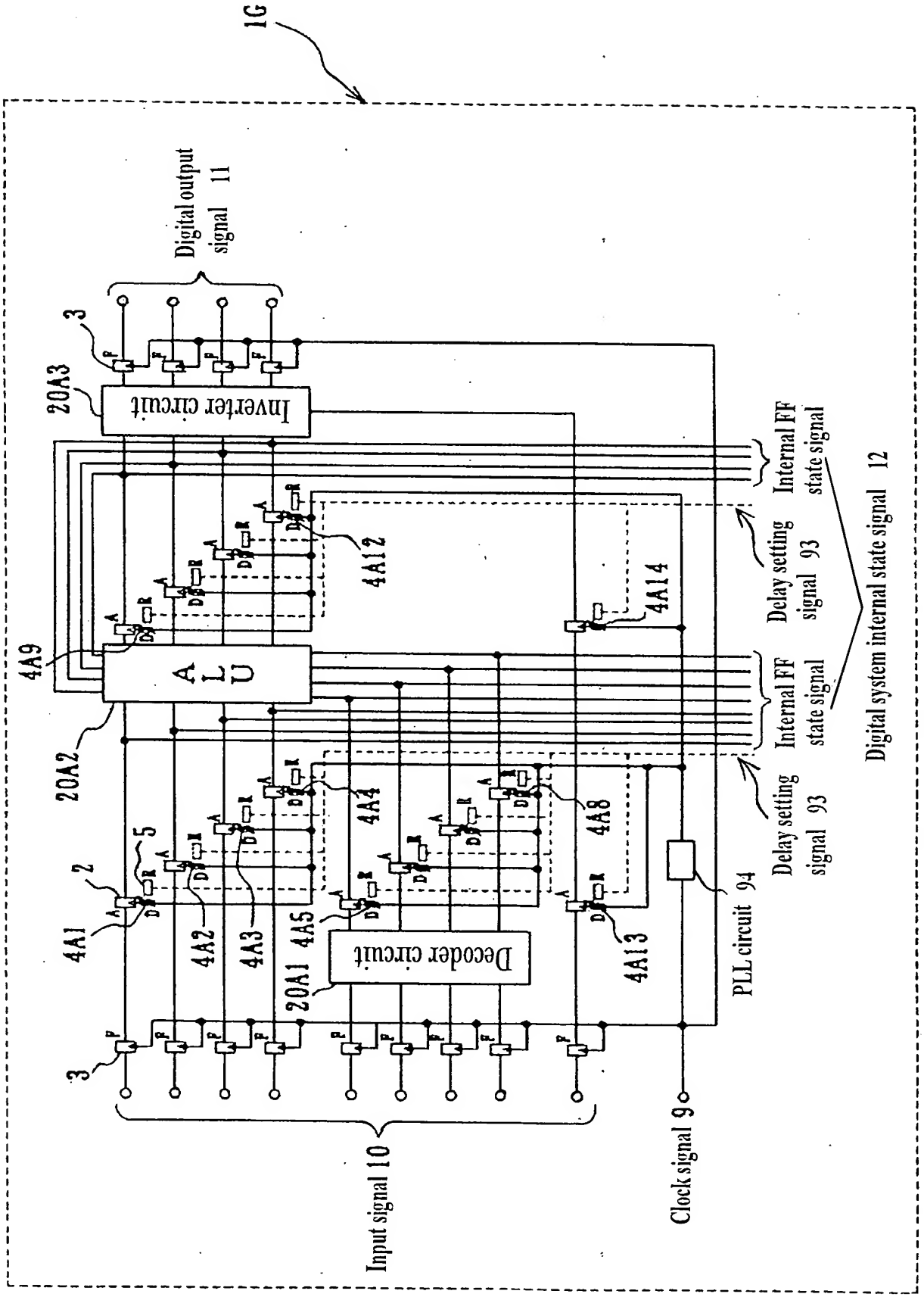

1G
Digital output signal 11
3
20A3
Inverter circuit
4A9
A L U
20A2
4A12
4A14
4A4
4A8
4A1
4A2
4A3
4A5
20A1
Decoder circuit
4A13
PLL circuit 94
Internal FF state signal
Delay setting signal 93
Digital system internal state signal 12
Input signal 10
Clock signal 9

FIG. 30

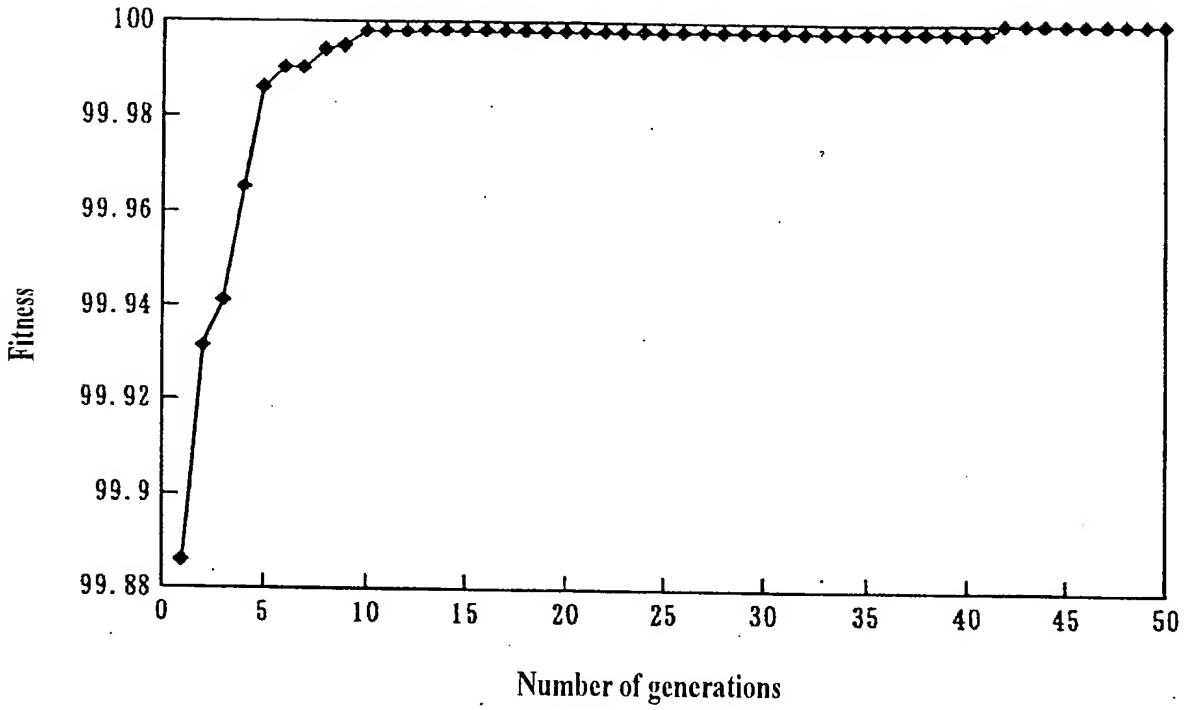

100
99.98
99.96
99.94
99.92
99.9
99.88
Fitness
0
5
10
15
20
25
30
35
40
45
50
Number of generations

FIG. 31

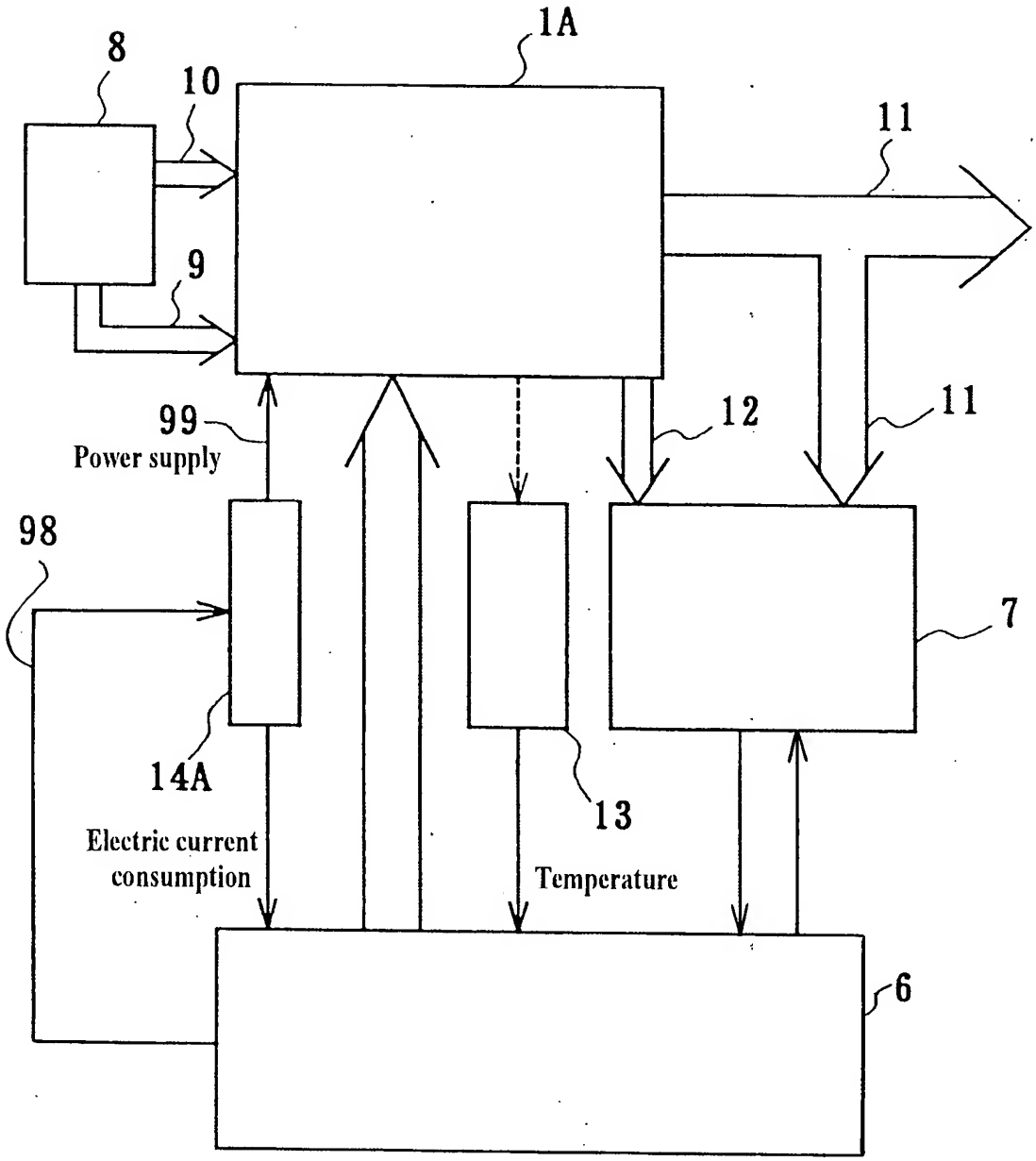

8
10
1A
11
9
99
Power supply
12
11
98
7
14A
13
Electric current consumption
Temperature
6

FIG. 32

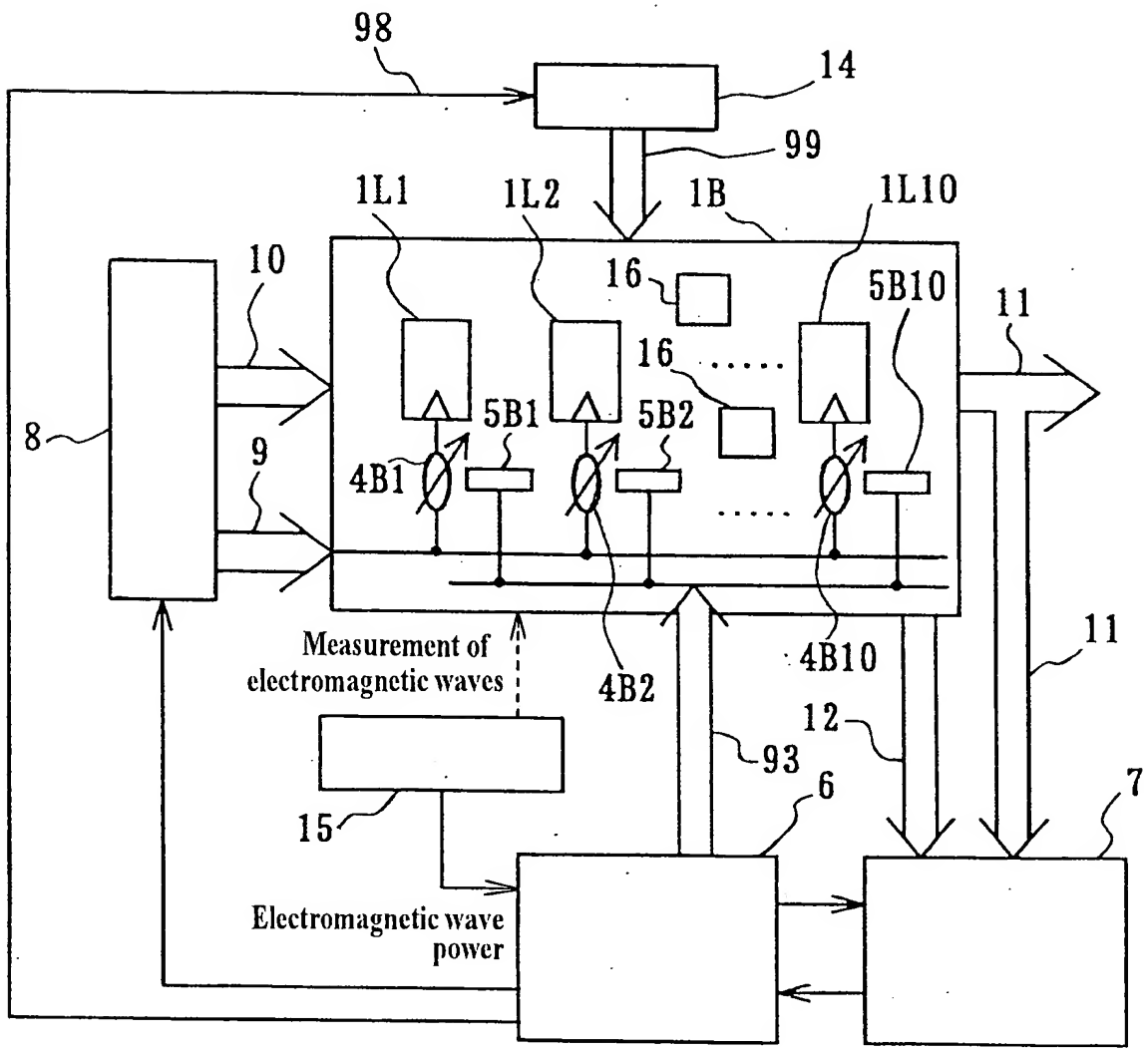

98
14
99
1L1
1L2
1B
1L10
10
16
5B10
11
16
5B1
5B2
8
9
4B1
Measurement of
electromagnetic waves
4B2
4B10
11
12
93
6
7
15
Electromagnetic wave
power

FIG. 33

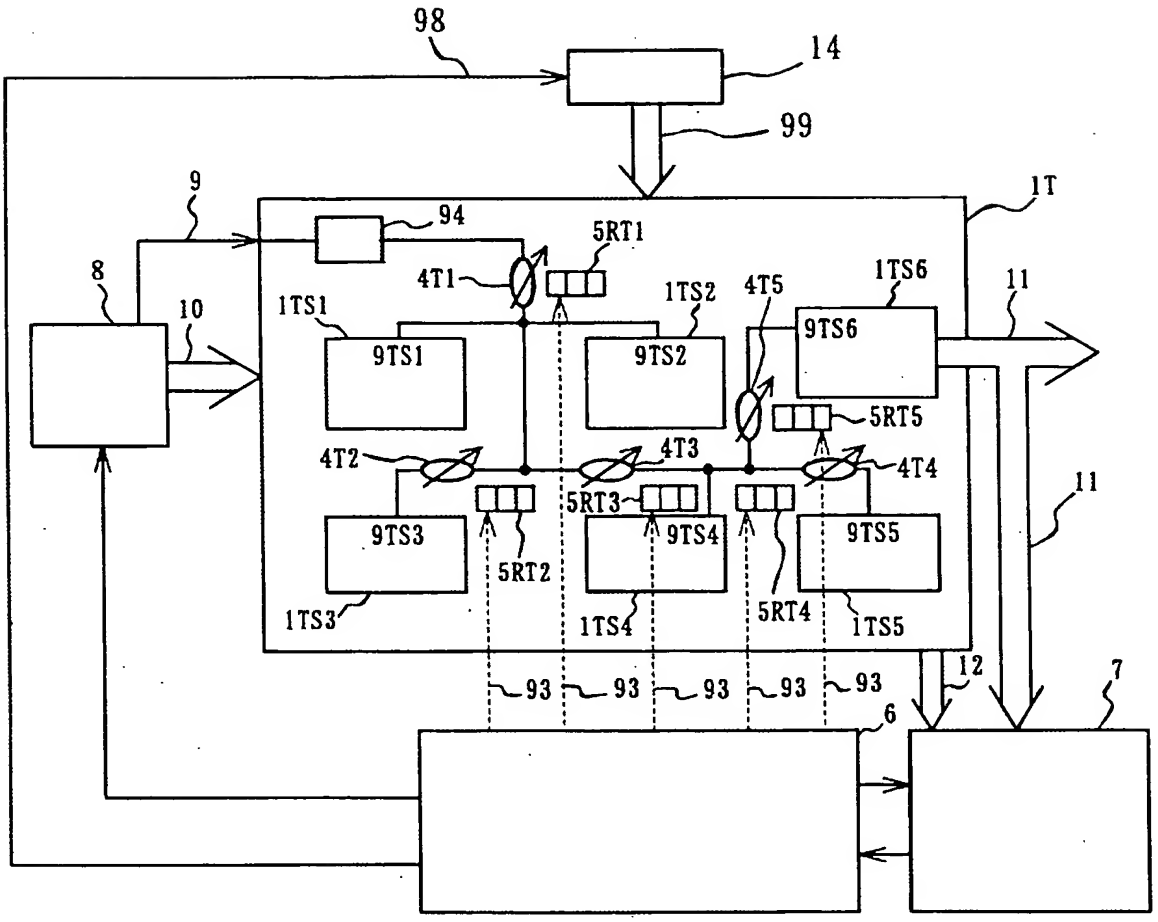

98
14
99
9
1T
94
5RT1
4T1
8
10
1TS1
1TS2
4T5
1TS6
11
9TS1
9TS2
9TS6
5RT5
4T2
4T3
4T4
11
5RT3
9TS3
5RT2
9TS4
9TS5
1TS3
1TS4
5RT4
1TS5
12
7
93
93
93
93
93
6

FIG. 34

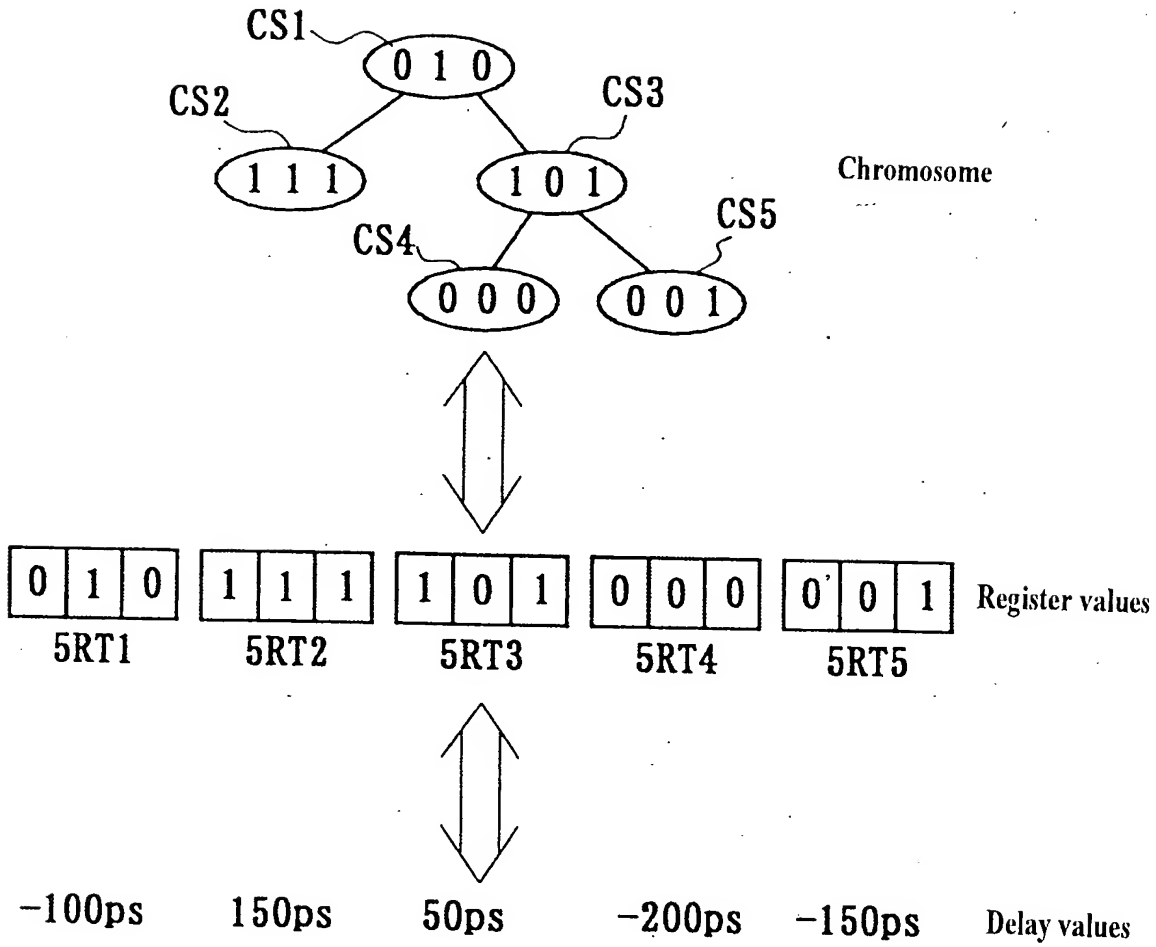

CS1
0 1 0
CS2
CS3
1 1 1
1 0 1
Chromosome
CS4
CS5
0 0 0
0 0 1
0 1 0
1 1 1
1 0 1
0 0 0
0 0 1
Register values
5RT1
5RT2
5RT3
5RT4
5RT5
-100ps
150ps
50ps
-200ps
-150ps
Delay values

FIG. 35

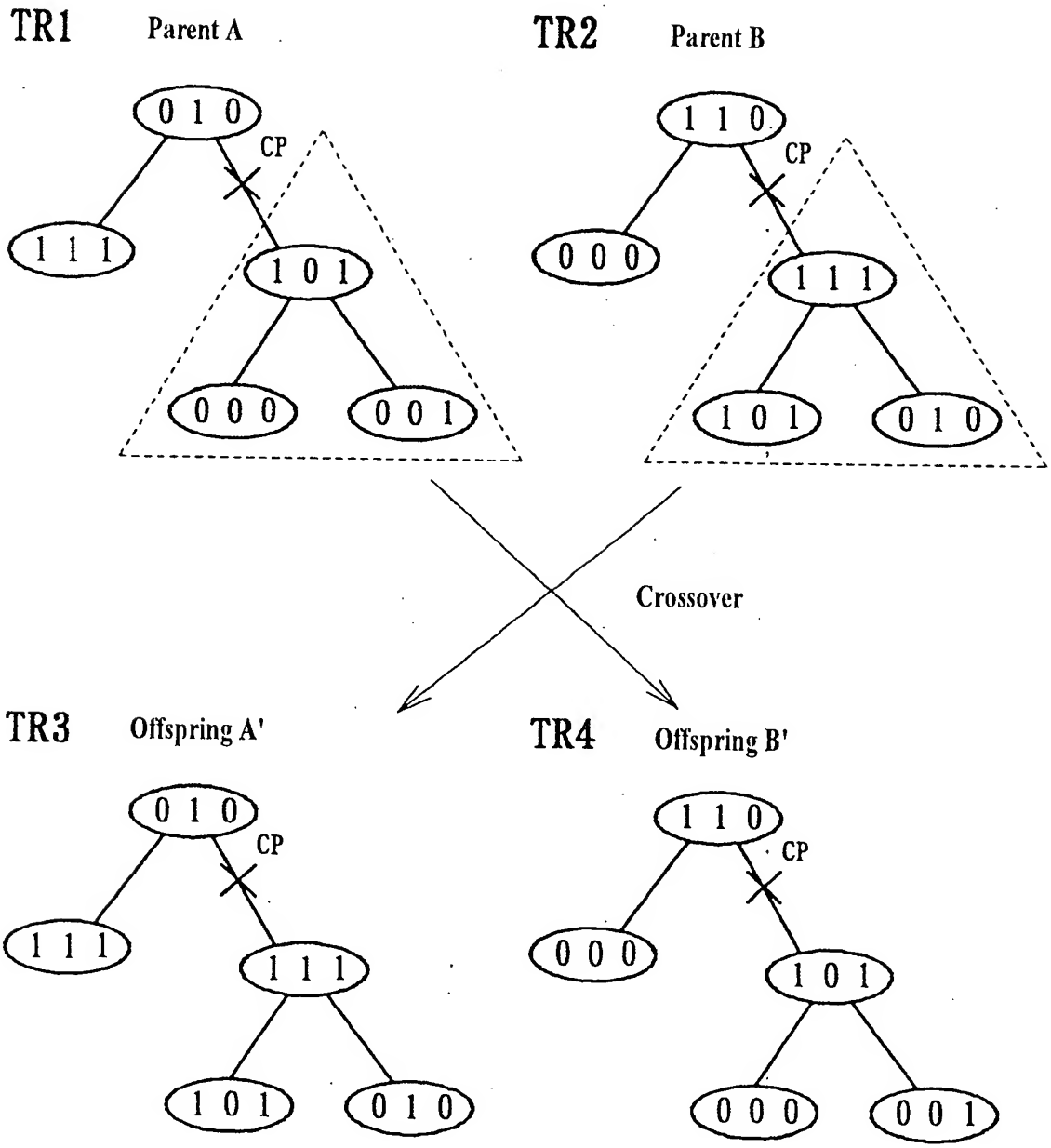

TR1
Parent A
0 1 0
CP
1 1 1
1 0 1
0 0 0
0 0 1
TR2
Parent B
1 1 0
CP
0 0 0
1 1 1
1 0 1
0 1 0
Crossover
TR3
Offspring A'
0 1 0
CP
1 1 1
1 1 1
1 0 1
0 1 0
TR4
Offspring B'
1 1 0
CP
0 0 0
1 0 1
0 0 0
0 0 1

FIG. 36